UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,738	07/14/2003	Sabhapathi N. Annamaneni	22272-08030	7030

758 7590 03/07/2007	EXAMINER	
FENWICK & WEST LLP	ORTIZ RODRIGUEZ, CARLOS R	
SILICON VALLEY CENTER		
801 CALIFORNIA STREET	ART UNIT	PAPER NUMBER
MOUNTAIN VIEW, CA 94041	2125	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

	Application No.	Applicant(s)
Office Action Summary	10/619,738	ANNAMANENI ET AL.
	Examiner	Art Unit	
	Carlos Ortiz-Rodriguez	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *14 March 2006*.
2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-57* is/are pending in the application.
   4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) *1-57* is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a) ☐ All   b) ☐ Some * c) ☐ None of:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. _____.
    3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date *12/30/04, 01/24/05, 03/14/06.*
4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2.   Claims 1-21, 23-24, 26-28, 30-49, 51-52 and 54-56 are rejected under 35 U.S.C. 102 (b)

as being anticipated by Burdick et al. U.S. Patent No. 5,889,674.

Regarding claims 1 and 30 Burdick et al discloses a system/method for identifying

transactions from WIP status updates, the system/method comprising: an adaptor (FIG 5

elements 505, 506, 507 and 508) for receiving WIP status updates for a semiconductor product

from at least one supplier in a supply chain for the semiconductor product (C9 L52-67); and a

transaction identifier (FIG 5 element 509) coupled to the adapter for identifying transactions

based on a comparison of the WIP status updates with a previous WIP status for the

semiconductor product (C10 L1-3).

Regarding claim 2 Burdick et al discloses receiving WIP status updates comprises:

receiving the WIP status updates from a single supplier (C1 L15-26).

Regarding claims 3 and 31 Burdick et al discloses receiving WIP status updates

comprises: receiving the WIP status updates from at least two different suppliers (C1 L15-26).

Regarding claims 4 and 32 Burdick et al discloses converting the WIP status updates to a

generalized form (C3 L5-17), wherein the step of identifying transactions based on a comparison

comprises identifying transactions based on a comparison of the WIP status updates in the

generalized form with the previous WIP status for the semiconductor product (C3 L22-25 and C4

L51-64).

Regarding claims 5 and 33 Burdick et al discloses converting the WIP status updates to a

generalized form comprises: converting all WIP status updates to the generalized form (C4 L51-

64 and C5 L17-25).

Regarding claims 6 and 34 Burdick et al discloses receiving WIP transactional updates

for the semiconductor product from at least one supplier in the supply chain for the

semiconductor product; and converting the WIP transactional updates to the generalized form

(C4 L51-64).

Regarding claims 7 and 35 Burdick et al discloses generalized form identifies a

processing status of the semiconductor product according to a predefined set of logical

operations that describe the supply chain (C3 L18-21 and C4 L1-14).

Regarding claims 8 and 36 Burdick et al discloses, for at least one supplier, the WIP status updates received from that supplier identify a processing status of the semiconductor product according to processing steps, and the processing steps have a finer granularity than the logical operations in the predefined set (C4 L15-40).

Regarding claims 9 and 37 Burdick et al discloses identifying transactions based on a comparison comprises: identifying supply chain events based on a comparison of the WIP status updates with the previous WIP status for the semiconductor product; and interpreting the supply chain events as transactions (C7 L1-10 and C9 L52-67 and C10 L1-3).

Regarding claims 10 and 38 Burdick et al discloses interpreting the supply chain events as transactions comprises: creating transient WIP status if a supply chain event is interpreted as at least two transactions (C9 L64-66).

Regarding claims 11 and 39 Burdick et al discloses that the WIP status updates are expressed in lots, each lot containing a quantity of the semiconductor product; and the step of identifying transactions occurs on a lot basis (C9 L64-67).

Regarding claims 12 and 40 Burdick et al discloses the transactions are selected from a predefined group that includes: a start transaction, a move transaction, a merge transaction, a split transaction, a scrap transaction, a bonus transaction, and an update transaction (C10 L1-3

and C13 L1-22).

Regarding claims 13 and 41 Burdick et al discloses identifying transactions comprises: identifying transactions based on a change in the quantity of semiconductor product in a lot (Claim 1).

Regarding claims 14 and 42 Burdick et al discloses identifying transactions comprises: grouping lots from the WIP status update with lots from the previous WIP status; and identifying transactions within the groupings (Claim1).

Regarding claims 15 and 43 Burdick et al discloses grouping lots is based on a customer product ID (Claim 1).

Regarding claims 16 and 44 Burdick et al discloses grouping lots is based on a main lot ID (Claim 1).

Regarding claims 17 and 45 Burdick et al discloses grouping lots is based on a customer lot ID (Claim 1).

Regarding claims 18 and 46 Burdick et al discloses identifying transactions within the groupings comprises: classifying lots according to a change in the quantity of the lot from the previous WIP status to the WIP status update; and identifying transactions by combining lots

according to their classifications (Claim 1).

Regarding claims 19 and 47 Burdick et al discloses identifying transactions within the

groupings comprises: classifying lots according to a change in the quantity of the lot from the

previous WIP status to the WIP status update; identifying possible valid combinations of lots

according to their classifications; and identifying transactions by evaluating the possible valid

combinations of lots (Claim 1, C9 L65-67, C10 L1-3 and Fig 4A).

Regarding claims 20 and 48 Burdick et al discloses identifying transactions within the

groupings comprises: classifying lots according to a change in the quantity of the lot from the

previous WIP status to the WIP status update, including classifying lots as quantity gaining lots,

quantity losing lots, potential split-child lots and potential merge-child lots; identifying possible

split events as valid combinations of quantity losing lots with potential split-child lots;

identifying possible merge events as valid combinations of quantity gaining lots with potential

merge-child lots; identifying possible valid combinations of possible merge events and possible

split events; and identifying transactions by evaluating the possible valid combinations of

possible merge events and possible split events (Claim 1, C9 L65-67, C10 L1-3 and Fig 4A).

Regarding claims 21 and 49 Burdick et al discloses identifying transactions comprises:

accessing a set of rules governing an identification of transactions; and applying the rules to the

WIP status updates and the previous WIP status (C9 L60-63 and C8 L20-22).

Regarding claims 23 and 51 Burdick et al discloses updating the previous WIP status for

the semiconductor product based on the transactions (C10 L1-3, C6 L8-19 and Claim1).

Regarding claims 24 and 52 Burdick et al discloses making reports of the updated WIP

status available to a customer (C8 L56-58 and C7 L8-10).

Regarding claims 26 and54 Burdick et al discloses processing the transactions to update a

transactional enterprise system (C13 L37-58).

Regarding claims 27 and 55 Burdick et al discloses that the transactional enterprise

system is an MES, an ERP, or a SCM system (C9 L64-67).

28 and 56. The method of claim 26 further comprising: updating the previous WIP status for the

semiconductor product based on the updated transactional enterprise system (C9 L64-67).

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

4.   Claims 22, 25, 50 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Burdick et al. U.S. Patent No. 5,889,674 in view of "Oracle E-Business Suite High-Tech

Semiconductor Industry Solutions, Achieving Excellence in Manufacturing and Customer

Response Through Oracle Shop Floor Management" (An Oracle White Paper, February 2003).

Regarding claim 22, 25, 50 and 53 Burdick et al. discloses all the limitations of the base

claims.

But Burdick et al. fails to clearly specify that identifying transactions comprises: defining

a priority among transactions; and generating a notification if at least two possible transactions of

equal priority can be identified from the same WIP status update(s) and that receiving WIP status

updates for a semiconductor product from at least one supplier comprises: intercepting at least

one WIP status update transmitted by one of the suppliers to a customer before the WIP status

update reaches the customer.

However, Burdick et al. in combination with "Oracle E-Business Suite High-Tech

Semiconductor Industry Solutions, Achieving Excellence in Manufacturing and Customer

Response Through Oracle Shop Floor Management", disclose that identifying transactions

comprises: defining a priority among transactions; and generating a notification if at least two

possible transactions of equal priority can be identified from the same WIP status updates

(Oracle E-Business Suite, High-Tech Semiconductor Industry Solutions, Achieving Excellence

in Manufacturing and Customer Response Through Oracle Shop Floor Management, Page 7,

Section: Shop Floor Move Transaction) and receiving WIP status updates for a semiconductor

product from at least one supplier comprises: intercepting at least one WIP status update

transmitted by one of the suppliers to a customer before the WIP status update reaches the

customer (Oracle E-Business Suite High-Tech Semiconductor Industry Solutions, Achieving

Excellence in Manufacturing and Customer Response Through Oracle Shop Floor Management,

Page 8, Section: "Lot Genealogy").

Therefore at time the invention was made, it would have been obvious to a person of

ordinary skill in the art to modify the above invention suggested by Burdick et al. and combining

it with the invention disclosed by "Oracle E-Business, Suite High-Tech Semiconductor Industry

Solutions, Achieving Excellence in Manufacturing and Customer Response Through Oracle

Shop Floor Management", the results of this combination would lead to system and method for

automating integration of semiconductor work in process updates.

One of ordinary skill in the art would have been motivated to do this modification

because in order to provide flexible tracking of every transaction that happens in a shop floor so

that customers could be notified as suggested by Oracle E-Business Suite High-Tech

Semiconductor Industry Solutions, Achieving Excellence in Manufacturing and Customer

Response Through Oracle Shop Floor Management.

5.   Claims 29 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burdick

et al. U.S. Patent No. 5,889,674 in view of Yang et al. U.S. Pub. No. 2003/0236718.

Regarding claims 29 and 57 Burdick et al. discloses all the limitations of the base claims.

But Burdick et al. fails to clearly specify wherein the transactions are compatible with

RosettaNet.

However, Burdick et al. in combination with Yang et al. disclose wherein the transactions

are compatible with RosettaNet (Yang et al. Claim 23).

Therefore at time the invention was made, it would have been obvious to a person of

ordinary skill in the art to modify the above invention suggested by Burdick et al. and combining

it with the invention disclosed by Yang et al.

One of ordinary skill in the art would have been motivated to do this modification in

order to provide semiconductor manufacturing industry wide standardization as suggested by

Yang et al.

Citation of Pertinent Prior Art

6.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure. The following patents are cited to further show the state of the art with respect to

system and method for automating integration of semiconductor work in process updates:

a. U.S. Patent No. 5,751,581 to Tau et al., which discloses material movement server.

b. U.S. Patent No. 5,841,660 to Robinson et al. which discloses method and apparatus

for modeling process control.

c. U.S. Patent No. 6,684,121 to Lu et al., which discloses real time work-in-process

(WIP) system.

d. U.S. Patent No. 6,748,287 to Hagen et al. which discloses adaptive real-time work-in-

progress tracking, prediction, and optimization system for a semiconductor supply chain.

e. U.S. Patent No. 6,839,601 to Yazback et al., which discloses fabrication architecture

including enterprise resource planning integration.

f. U.S. Patent No. 6,871,113 to Maxim et al., which discloses real time dispatcher

application program interface.

g. U.S. Patent No. 6,959,226 to Hseih, which discloses system and method for split lot id naming.

h. U.S. Patent No. 7,006,885 to Chen, which discloses method for generating a suggestive dispatch upstream/downstream stage requirements.

The following publications are cited to further show the state of the art with respect to system and method for automating integration of semiconductor work in process updates:

i. U.S. Pub. No. 2002/0188682 to Jaln et al., which discloses method and system for manufacturing supply chain collaboration.

j. U.S. Pub. No. 2004/0001619 to Tai et al., which discloses an automatic intelligent yield improving and process parameter multivariate system and the analysis method thereof.

k. "A framework for supply chain management in semiconductor manufacturing industry", to Ovacik et al., i2 Technologies, 1995 IEEE.

l. "Oracle E-Business Suite High-Tech Semiconductor Industry Solution, Key SCM Challenges and Oracle's Strategy/Response", An Oracle White Paper, February 2003.

m. "eSilicon Delivers ASIC Time to market breakthrough; fables ASIC Company Announces Infrastructure to speed design, manufacture, and delivery of chips", Business Wire, July 24, 2001.
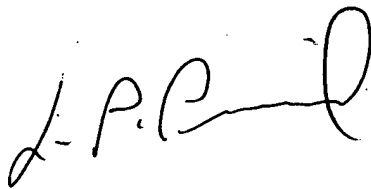
Conclusion

7.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Carlos Ortiz-Rodriguez whose telephone number is 571-272-

3677.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Carlos Ortiz-Rodriguez
Patent Examiner
Art Unit 2125

March 1, 2007

**LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100**